A Capacitive Pressure Sensor with Low Impedance Output and Active Suppression of Parasitic Effects

B PUERS, E PEETERS, A VAN DEN BOSSCHE and W SANSEN
Katholieke Universiteit Leuven, Electronics Department, ESAT Division, Kardinaal Mercierlaan 94, B-3030 Heverlee (Belgium)

Abstract

This paper describes the design, operating principles and performance of a capacitive pressure sensor in silicon, combined with a dedicated CMOS interface circuit The readout circuit is designed to suppress parasitics and to yield an output signal proportional to pressure The sensor-specific part is fabricated using standard photolithography, silicon micromachining in KOH, and anodic silicon/glass bonding at wafer level The devices measure 2 2 × 3 5 × 0 8 mm and show a typical zero-pressure capacitance of 10 pF, with pressure-induced changes up to 250%

The interface chip 'CAPRICE' (CApacitive Pressure sensor Readout IC) is processed in a 3 μm n-well CMOS process and was designed to anticipate the intrinsic drawbacks of the capacitive transducing principle, i e sensitivity to environment noise, nonlinear output response and effects of parasitic capacitances These drawbacks have always prevented the breakthrough of integrated capacitive mechanical sensors CAPRICE, however, converts small capacitance variations into a noise-insensitive output voltage and a first-order linearisation is achieved by inversion of the hyperbolic capacitance versus pressure relationship A second-order linearisation is obtained by the adoption of a novel suppression scheme for parasitic capacitances to the substrate Parasitic capacitance rejection ratios up to 80 dB can be achieved in this way, enabling the practical feasibility of capacitive pressure sensors with less than 0 5% of full-scale nonlinearity

1. Introduction

Most of the comparative studies that have been published [1–3] agree on the issue that integrated capacitive mechanical sensors offer much higher potentials than their piezoresistive counterparts as far as sensitivity, temperature behaviour, stability and power consumption are concerned Devices exhibiting all of these qualities would particularly be suited for the most demanding applications, such as those in the biomedical world Sensor stability and power consumption are crucial factors in the case of a long-term medical implant Capacitive devices can outrun the piezoresistive devices by orders of magnitude for both specifications Yet, no breakthrough of a capacitive sensor has been seen in this field so far, despite years of effort Moreover, research on capacitive pressure sensors and accelerometers has been conducted for just as long as on piezoresistive devices [2] Yet, hardly any commercial pressure sensor of the capacitive type is available, while the resistive ones are widespread

An explanation for these contradictions is that the exploitation of the large potential qualities of highly miniaturised capacitive sensors is often inhibited by the presence of parasitic effects, such as environment noise, parasitic capacitances and leakage resistors They severely decrease the sensor performance, whereas the effect on the resistive devices is much less pronounced Noise pick-up and nonlinearity are particularly problematic for capacitive microsensors

The mentioned parasitic effects are of a fundamental nature and are inherently related to miniaturisation in the case of a capacitive device Downscaling of the sensor dimensions implies downscaling of the active capacitance values Thus, full integration implies active sensing capacitances that are only in the pF range Hence, high output impedances and noise sensitivity cannot be avoided and the effects of stray capacitances become dramatic The only way to cope with these difficulties is to incorporate a dedicated readout circuit inside the sensor package

This paper reports on the realisation of a capacitive-type silicon pressure sensor designed for biomedical application [4] The typical sensor-related problems are pointed out and the interface circuit to handle them, CAPRICE (CApacitive Pressure sensor Readout Integrated Circuit), is described CAPRICE performs an adequate sup-

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pression of the parasitics and the realisation of a capacitive transducer with less than 0 5% of FS (full-scale) nonlinearity is made practically feasible for the first time

2. Structure and Fabrication of the Pressure Sensor

As shown schematically in Fig 1, the sensors basically consist of a glass/silicon sandwich with overall dimensions of $2\,2 \times 3\,5 \times 0\,8$ mm The starting material for the fabrication is a 3 in type double-side polished silicon wafer with a p-type epitaxial layer

First, the reference cavity that determines the capacitor plate separation is etched on the epi side of the wafer A wet isotropic etch in $HNO_3/BHF/H_2O$ and photoresist as the masking material is sufficient for this purpose An ultrasonic etch bath is used to improve the etch rate uniformity A typical cavity depth or zero-pressure plate separation lies between 1 and 2 μm Hence, the zero-pressure capacitance C_0 lies in the order of 10 pF Secondly, the membrane capacitor plate is defined in the reference cavity by an arsenic ion implantation

After a double-sided alignment, the pressure-sensing membranes are formed in the silicon wafer by an anisotropic etch from the backside The thickness of the diaphragm is accurately controlled by the application of a two-electrode p–n junction etch-stop technique in a KOH/H_2O solution [5] The membrane thickness ranges from 5 to 20 μm, yielding a typical pressure range from 100 to 1500 hPa [6]

A sputter-deposited layer of Ti/Pt (100 nm) on the 3 in borosilicate glass wafer serves as the top capacitor plate Later on, the silicon is anodically bonded [7] to the glass at wafer level Dicing in individual devices is the last step in the fabrication sequence

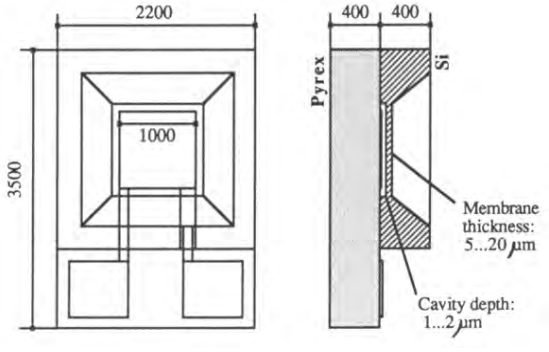

Fig 1 A schematic presentation of the fabricated capacitive pressure sensor

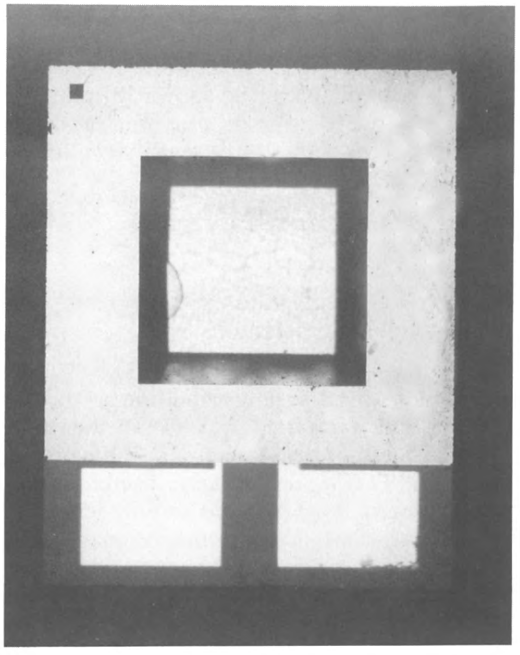

Fig 2 Microphotograph of a completed sensor device

Figure 2 is a photograph of a finished sensor device The large bondpads enable direct lead soldering

3. Measurements

Figure 3 presents measured pressure characteristics of the described microsensor Note the very high pressure sensitivity the capacitance change induced by the full-scale pressure is higher than 100% of the zero-pressure capacitance This capacitance swing is to be compared with a 5% swing or less for a piezoresistive device

Excellent temperature behaviour is known to be another specific merit of a capacitive transducing principle [1–3] However, the reference cavity

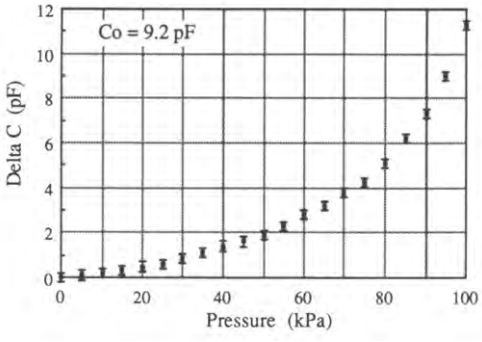

Fig 3 Measured capacitance vs pressure characteristics

of the sensor in Fig 2 was sealed under ambient pressure Thermal expansion of the trapped gas is responsible for the high temperature coefficients that were measured It can be shown [8] that the TCO (temperature coefficient of offset) and the TCS (temperature coefficient of sensitivity) due to thermal gas expansion, are given by

$$(TCO)_g = -(P_{seal}/T_{seal}) \quad (1)$$

$$(TCS)_g = -0\,5(P_{seal}/P_{max})\ (1/T_{seal}) \quad (2)$$

where T_{seal} = seal temperature, P_{seal} = seal pressure, P_{max} = full-scale pressure

i e , $(TCO)_g = -175$ Pa/°C and $(TCS)_g = -870$ ppm/°C for the given sealing conditions

However, the measured values for the total TCO and TCS are of the same order of magnitude as $(TCO)_g$ and $(TCS)_g$ respectively Therefore, the pressure sensor in Fig 2 would exhibit temperature coefficients that lie an order of magnitude below what was measured, if it were sealed under vacuum [3]

The frequency response was measured to be better than 1 kHz

4. Sensor-related Problems

The measured output impedance is typically as large as 300 MΩ at 50 Hz Therefore, the capacitive sensors are very susceptible to environmental noise and their application is restricted to very well shielded environments, unless an impedance conversion is performed inside the sensor package itself Nonlinearity is also a common drawback for pressure sensors of the capacitive type It is obvious that the sensing capacitance C_x can be expressed as

$$C_x = \iint_A \frac{\varepsilon_0\,dx\,dy}{d_0 - w(x,y)} \quad (3)$$

where A = area of the capacitor plates, d_0 = zero-pressure plate separation, $w(x, y)$ = local membrane deflection

This expression and the curve in Fig 3 suggest a hyperbolic relationship between the output capacitance and the applied pressure But even after inversion of this relationship, the remaining nonlinearity is larger than 10% of FS for the case in Fig 3 This can be noted in Fig 4, where V_{out} is proportional to the inverse of the sensor capacitance V_{out} in this Figure is the measured output voltage of a breadboarded capacitance to voltage convertor that performs the inversion The nonlinearity of V_{out} versus P_x is 12% of FS This nonlinear behaviour is a common feature for all capacitive sensors of this kind and is mainly caused by two reasons

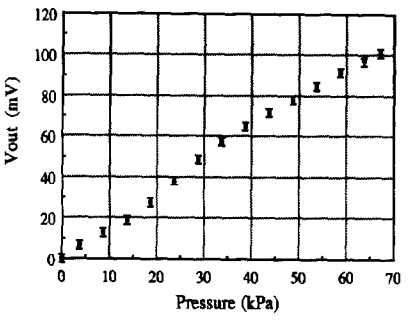

Fig 4 Measured voltage vs pressure relationship after a first-order linearisation Note the typical 'S' shape

The first reason is mechanical in nature Deformation of the membrane capacitor plate as the membrane flexes causes a deviation from a perfect hyperbolic relationship The phenomenon manifests itself in Fig 4 as a saturation effect in the higher part of the pressure range However, this component of nonlinearity can be avoided by the adoption of a membrane type with a stiffened central area to keep both capacitor plates parallel for the entire pressure range [6]

The second reason is electrical in nature The presence of parasitic or stray capacitances causes the total capacitance ($C_{tot} = C_x + C_p$) to be only partly sensitive to pressure These parasitic capacitances become relatively more important for smaller values of the sensing capacitance C_x, i e for smaller applied pressures Hence, the sensor characteristics will be distorted in the lower part of the pressure range, as can be seen in Fig 4

Leakage resistors over the sensor capacitor and electrostatic pressure [9] also contribute to nonlinearity, but the effects can be kept of much less importance by fast sampling and reduction of voltage over the sensing capacitor

5. Requirements and Functional Description of the Signal Conditioning Circuit CAPRICE

As pointed out in the previous paragraph, the objective of an interface circuit for miniature capacitive pressure sensors should be three-fold The following issues are important in order to enable the fabrication of a linear and noise-insensitive transducer First, a conversion to a low impedance output is imperative Secondly, a first-order linearisation should be achieved by inversion of the capacitance versus pressure relationship, in combination with sensors of the stiffened membrane type Thirdly, parasitic capacitances, leakage resistors electrostatic pressure must be thoroughly suppressed The CMOS circuit 'CAPRICE' that

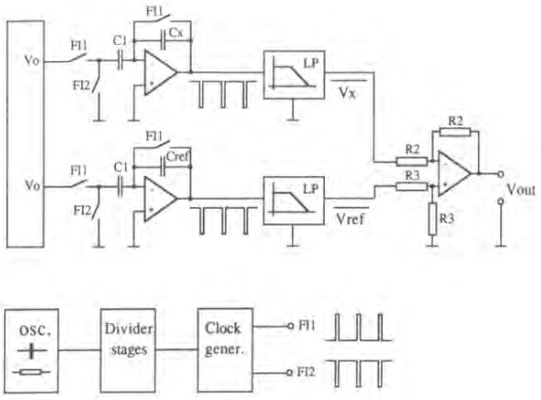

Fig 5 Functional overview of CAPRICE (CApacitive Pressure sensor Readout IC)

was designed and processed for this purpose, can accomplish all three objectives

Figure 5 shows a functional overview of the interface system CAPRICE is basically a switched capacitor [10] capacitance-to-voltage convertor in a differential measuring set-up The functioning is as follows

During clock phase FI1, the on-chip capacitors C_1 are charged to a reference voltage V_0, while the sensor capacitor C_x and the reference capacitor C_{ref} are discharged C_{ref} is a micromachined capacitor of the same type as C_x, but insensitive to pressure changes During phase FI2, the charge on C_1 is transferred to the sensor C_x and to the reference capacitor C_{ref}, to yield the voltages V_x and V_{ref} after low-pass filtering The clock phases were chosen to be asymmetrical in order to enable their removal from the output by a simple filtering technique Consequently, a d c voltage level is present at the output of the filters

$$V_x = V_0 C_1 (1/C_x) \tag{4}$$

$$V_{ref} = V_0 C_1 (1/C_{ref}) \tag{5}$$

Finally, the output voltage is obtained from a differential amplifier (amplification A_D)

$$V_{out} = A_D V_0 C_1 [(1/C_{ref}) - (1/C_x)] \tag{6}$$

The output voltage is proportional to the difference of the inverses of capacitors C_{ref} and C_x This is essential when an output signal proportional to pressure is required, as will be shown in the next Section

CAPRICE was processed in a 3 μm n-well CMOS process and it measures 1 6 × 2 5 mm Figure 6 is a microphotograph of the circuit The numerous bondpads are to provide testability No external components are required

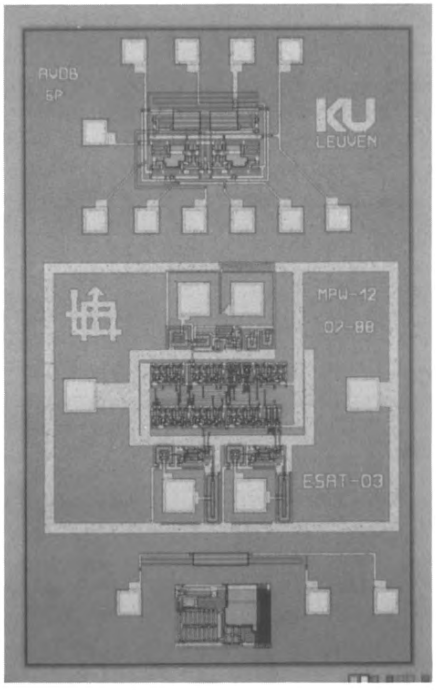

Fig 6 Microphotograph of the CAPRICE interface chip

6. First-order Linearisation

In general, the output capacitance of a sensor as in Fig 1, is given by expression (3) However, in a configuration with a stiffened membrane as in Fig 7, eqn (3) reduces to [11]

$$C_x = \frac{\varepsilon_0 A}{d_0 - kP_x} \tag{7}$$

with k a constant, depending on membrane geometry and dimensions

If the membrane thickness is chosen in such a way that both capacitor plates make mechanical contact at the maximum of the pressure range, the following relation holds

$$kP_{max} = d_0 \tag{8}$$

Furthermore, the value of the reference capacitor C_{ref} in Fig 5 is chosen to equal the zero-pressure

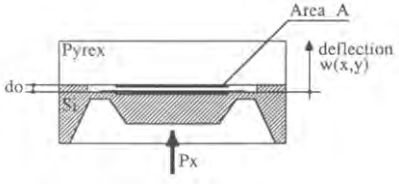

Fig 7 Cross section of a capacitive pressure sensor with a centrally stiffened membrane

capacitance of the sensor

$$C_{ref} = C_0 = \varepsilon_0 A/d_0 \tag{9}$$

The combination of eqns (7), (8) and (9) yields

$$C_x = \frac{C_{ref}}{1-(P_x/P_{max})} \tag{10}$$

Finally, the output voltage of CAPRICE as a function of applied pressure, is obtained from eqns (10) and (6)

$$V_{out} = A_D V_0 (C_1/C_{ref})(P_x/P_{max}) \tag{11}$$

Consequently, in the absence of parasitic effects, CAPRICE in combination with a stiffened membrane-type sensor, will yield at low impedance output voltage that is proportional to pressure

7. Second-order Linearisation

In a practical situation, however, the presence of parasitic capacitances cannot be avoided Figure 8 shows a typical situation

$$C_{tot} = C_x + C_p \tag{12}$$

$$C_p \cong C_{p3} + C_{p1}C_{p2}/(C_{p1} + C_{p2}) \tag{13}$$

C_{p1} and C_{p2} are parasitic capacitances to the silicon substrate, while C_{p3} is a direct shunt capacitance However, C_{p1} and C_{p2} are connected in series through the resistance of the substrate and are thus added to the shunt C_{p3} (see expression (13))

The stray capacitance C_{p3} can be kept small compared to C_x by careful sensor layout, provided that the interface chip is placed very close to the sensor device (capacitance between leads or bondwires adds up in C_{p3}) C_{p1} and C_{p2}, however, can be even larger than the sensing capacitance itself C_{p1} could be the capacitance between an interconnect line, through the isolating oxide layer, to the substrate and could easily be in the order of a few pFs Fringing fields contribute to C_{p2} if the substrate is biased, as in Fig 9 In that case, however, C_{p2} mainly consists of the space charge capacitance of the inversely polarised p–n junction that isolates the ion-implanted membrane electrode from the substrate Depending on the sensor dimensions, this capacitance can range up to 100 pF and it is voltage dependent

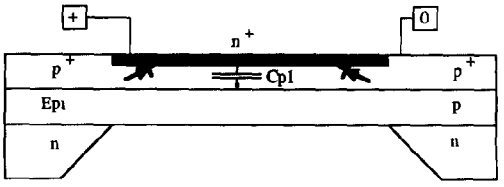

Fig 9 Cross section of the sensor membrane with substrate biasing

Anyhow, it is extremely difficult to reduce the value of the total parasitic capacitance below the order of a few pFs by means of sensor topology or construction only It is impossible altogether when a double silicon sandwich structure is used instead of the Si/glass sandwich, as in Fig 1 The double silicon approach offers interesting potentials though, as far as sensor stability, temperature sensitivity and CMOS compatibility are concerned [11] Figure 10 demonstrates that even a few pFs of stray capacitance have a large impact on the linearity and sensitivity of the transducer and hence cannot be tolerated

Therefore, CAPRICE features a suppression mechanism for parasitics Such a suppression can readily be achieved in the scheme of Fig 5 by connecting the sensor substrate to ground The situation that occurs in that case is depicted in Fig 11

C_{p1} merely acts as an extra load capacitance for the operational amplifiers and theoretically does

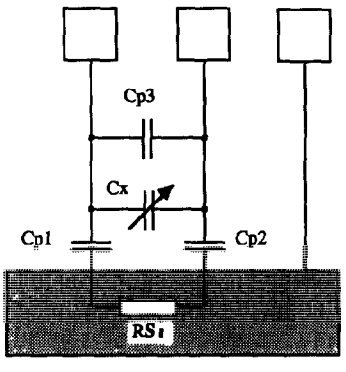

Fig 8 Schematic presentation of the sensing capacitor with the two kinds of parasitic capacitances

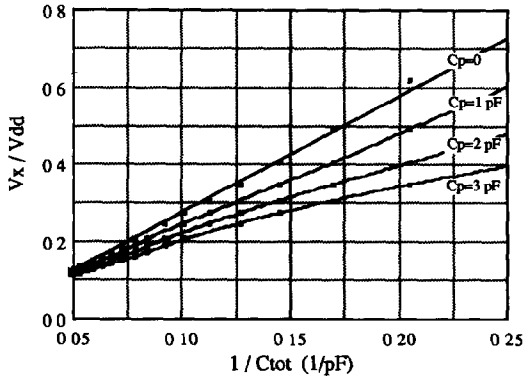

Fig 10 The effect of parasitic capacitance on the sensor characteristics in a floating configuration

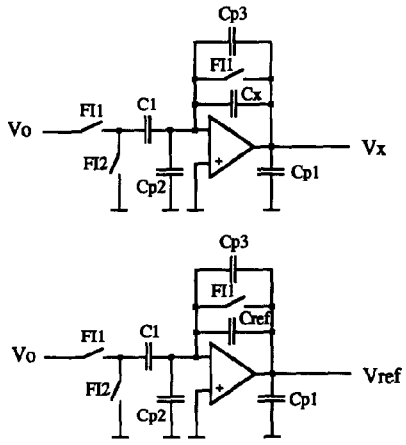

Fig 11 Location of the parasitic capacitances when the substrate is tied to ground

not influence the voltages V_x or V_{ref} (Fig 11), provided that the opamps were designed for the extra load (possibly up to 100 pF) C_{p2}, on the other hand, is connected between actual ground and virtual ground and will not contribute to any net charge transfer Therefore, it will not influence V_x or V_{ref} However, C_{p3} remains unsuppressed in the individual opamp stages, but it is small compared to C_x and it is therefore still adequately cancelled out in the differential measurement set-up

The suppression performance of CAPRICE in a practical situation is demonstrated in Fig 12 This Figure presents measured data, with the parasitic capacitance C_{p1} simulated by means of ceramic capacitors ranging from 1 to 300 pF The results are to be compared to Fig 10 The nonlinearity arising from the 300 pF 'parasitic' capacitance with the substrate tied to ground, is merely 0 03% of FS (Fig 12) The same nonlinearity is caused by only 30 fF in a floating substrate

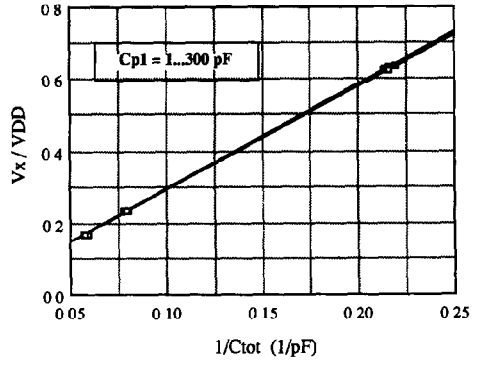

Fig 12 The effect of parasitic capacitance C_{p1} in a non-floating configuration

TABLE 1 Suppression specifications of CAPRICE

Parasitic scale capacitance	Suppression C_p(equiv) factor (dB)	C_p(typ) (pF)	Full-nonlinearity (%)	(fF)
C_{p1}	−80	200	0 02	20
C_{p2}	−50	10	0 03	30
C_{p3}		0 2	0 10	
Total			0 15	

TABLE 2 Overview of all CAPRICE specifications

Circuit specifications	Min	Typ	Max
Dimensions (mm)		1 6 × 2 5	
Supply voltage (V)	±1 5		±6
Supply current (μA)	50		1250
Sensitivity (V/V pF^{-1})	2 63	2 68	2 97
FS nonlin (%)			0 15
Temp sensitivity (ppm/°C)		−275	
PCRR C_{p1} (dB)		−80	
PCRR C_{p2} (dB)		−50	

configuration (Fig 10) A PCRR (parasitic capacitance rejection ratio) can then be defined as the ratio of the suppressed C_p over the unsuppressed C_p causing the same nonlinearity The PCRR for C_{p1} is −80 dB in the given example The suppression specifications for all three kinds of parasitic capacitances are summarised in Table 1

A concluding overview of all CAPRICE specifications is presented in Table 2 The low supply current, high sensitivity and low temperature sensitivity are to be noted, apart from the high linearity due to suppression of parasitics From this Table it can be concluded that the CAPRICE interface circuit has the ability to overcome the intrinsic drawbacks that have always prevented the breakthrough of miniature capacitive sensors, without sacrificing any of the specific merits of the capacitive transducing principle

8. Conclusions

Despite their obvious advantages and years of effort, hardly any integrated capacitive mechanical pressure sensors are commercially available at the time, while the piezoresistive counterpart is widespread It has been shown in this paper how the parasitic effects that have always obstructed the breakthrough of capacitive devices can be adequately suppressed by the introduction of a dedicated readout circuit inside the sensor package In a first stage, the realisation of a sensitive capacitive pressure sensor has been elaborated and the typical sensor related problems pointed out

Later, the interface chip 'CAPRICE' has been discussed CAPRICE suppresses parasitic capaci-

tances by up to 80 dB and enables the practical feasibility of linear, high-sensitivity capacitive pressure sensors for the first time

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